REMARKS/ARGUMENTS

The Applicants gratefully acknowledge the indication of allowable subject matter in claim 20. Reconsideration of the rejected claims is requested.

Claim 7 has been amended to correct the participle "a" to read "an" so that the claim is grammatically correct.

Claim 16 has been amended to add the word "which" after the word "at" so that the claim is grammatically correct.

Claim 23 has been amended to delete an extra comma.

All of these claim amendments have been made so that the claims are grammatically correct. The amendments make no substantive changes to the claims, and are not made to overcome prior art in any way.

Recitation of the Invention as-claimed:

One aspect of the invention, as recited in claim 1, is an imager system that is provided in a semiconductor substrate. The imager system includes a plurality of photosensitive, charge-integrating pixels that are arranged in rows and columns of a pixel array for capturing illumination of a scene to be imaged. Each pixel includes a photogenerated charge accumulation region of the substrate and a sense node at which an electrical signal, indicative of pixel charge accumulation, can be measured without discharging the accumulation region.

There is provided pixel access control circuitry that is connected to the pixel array rows and columns to deliver pixel access signals generated by the access control circuitry for independently accessing a selected pixel in the array.

An input interface circuit is connected to accept a dynamic range specification input for the array pixels. Integration control circuitry is configured to generate, based on the input dynamic range specification from the input

interface circuit, pixel-specific integration control signals to be delivered to a selected pixel, independent of other pixels. The integration control circuitry is connected to access a selected pixel of the array to read the sense node electrical signal of the selected pixel.

An output interface circuit is connected to the pixel array to produce output image data that is based on sense node electrical signals from the pixel array.

Rejections of the Claims:

Claims 1-5, 7-10, 14-19, and 21-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yanai et al., U.S. Patent No. 5,872,596 (hereinafter "Yanai").

Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yanai in view of Shinohara et al., U.S. Patent No. 5,587,738 (hereinafter "Shinohara").

Claims 11-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yanai in view of Lee et al. U.S. Publication 2002/0101528 (hereinafter "Lee").

The Applicants note that claims 1-18 are directed to an imager system, as recited in claim 1 and above; and claims 19 and 21-23 are directed to a method of controlling charge integration of pixels, as recited in claim 19 and below.

We first turn to the imager system of claims 1-18.

The Examiner suggested that Yanai describes an imager system provided in a semiconductor substrate as required by claim 1. This is not the case. In Yanai Figs. 1, 5, and 7, there is shown an "image pickup element 1" (col. 4, line 13) that communicates with an external microcomputer 14. Yanai's image pickup

element is said to include a photo cell 11 (Fig. 1) that stores an electric charge of one pixel of the image pickup element 1. Yanai's image pickup element therefore is understood to be an array of pixels provided in a semiconductor substrate. But Yanai's microcomputer clearly is not integrated with the image pickup element in a semiconductor substrate as required by the claims. Yanai explicitly points this out in Fig. 7 where an example image pickup sensor circuit, a BASIS circuit, is shown as one pixel of the pickup element 1. The microcomputer 14 is shown to be separate from the pixel by the dashed line around the pickup element. This separation of a microcomputer from a pickup element is universal to all Yanai's figures.

In contrast, the invention provides an imager system, not just an imaging pickup element, in a semiconductor substrate. Fig. 21 of the instant application is an example microchip layout for the monolithic integration of subsystems of an imager system in a semiconductor substrate in accordance with the invention. The inventors herein have discovered subsystem designs and microfabrication techniques that enable this monolithic integration of an imager system including pixels, pixel access control circuitry, input interface circuitry, integration control circuitry, and output interface circuitry as recited in claim 1.

The Applicants note that Lee, U.S. Patent Publication 2002/0101528 describes an "integrated CMOS image sensor," shown in Fig. 1 (col. 2, ¶19), and a camera employing the CMOS image sensor, shown in Fig. 3. But Lee does not teach or suggest provision of an imaging system in a semiconductor substrate as required by the claims. Instead, like Yanai, Lee employs a micro-controller 81 that is not integrated with an image sensor, and further employs an interface ASIC 82 that is not integrated with an image sensor. Neither Yanai nor Lee provides an enabling description or even a suggestion as to how subsystems of a full imager system could be provided together in a semiconductor substrate as required by the claims.

The Examiner suggested that Yanai's imager includes an array of charge integrating pixels, where each pixel includes a photogenerated charge accumulation region of a substrate and a sense node at which an electrical signal indicative of charge accumulation can be measured without discharging the accumulation region. The Applicants concur. But the Examiner pointed to Yanai reference numeral (13) as this pixel sense node. This is not correct; in Yanai Fig. 1, reference numeral (13) refers to "decision means," which appears to correspond to the comparator circuit of Yanai Fig. 27, as described at Yanai Col. 10, line 40, as "a comparator 18...." In Yanai Fig. 8, reference numeral (13) refers to "an output terminal of the solid-state image pickup element," (Col. 9, lines 56-57). Neither of these are Yanai's pixel sense node. Yanai's pixel sense node is, e.g., the emitter electrode e_2 of the transistor "bit S" of Yanai Fig. 7, (Col. 7, lines 1-8).

The Examiner pointed to Yanai's decision means 13 in Fig. 1 as a pixel sense node and pointed to Yanai Col. 4, lines 12-16 as describing a pixel having a sense node at which an electrical signal can be measured without discharge of the pixel. But this Yanai passage gives absolutely no description of pixel configuration, let alone a configuration that enables charge measurement without discharge. The passage states that when a signal amount stored in the photo cell exceeds a predetermined amount, the decision means generates a signal indicating the situation. No specific pixel architecture is described or can be implied from this passage.

The Examiner points to Yanai Col. 9, lines 49-53 as describing circuitry for accessing a selected pixel in Yanai's pixel array. The Applicants agree. But note that Yanai Fig. 8, in illustrating this circuitry, shows the access decoders separate from the pickup element 1. This indicates that Yanai's access circuitry is not integrated with the pixel array as required by the claims.

The Examiner pointed to Yanai's microcomputer 14 as integration control circuitry connected to access a selected pixel to read the sense node electrical

signal of the pixel. The Examiner suggested that Yanai's microcomputer 14 is configured to generate pixel-specific integration control signals delivered to a selected pixel, here referring to Yanai Col. 4, lines 16-19 and 25-31. These passages state that the microcomputer has a timer for measuring the that a stored pixel signal previously had reached a predetermined signal amount.

Yanai's microcomputer fails to meet requirements of the claims. First, as explained above, Yanai's microcomputer is not provided in a semiconductor substrate with a pixel array and other circuitry as required by the claims. Yanai's microcomputer is a separate, non-integrated element.

Further, the invention requires integration control circuitry that is connected to generate pixel-specific integration control signals based on a dynamic range specification input provided by an input interface circuit. In other words, the control circuitry is connected in the semiconductor substrate with the input interface circuit such that when a user inputs a dynamic range specification, the integration control circuitry generates a corresponding pixel-specific integration control signal. This aspect of the integration control circuitry recited in claim 1 was ignored by the Examiner. The Examiner is not permitted to ignore limitations of the claims, and must consider the invention as a whole, *MPEP 2141.02*.

Conventionally, at the time of the invention, it was understood that the dynamic range of an imager would typically be fixed. A conventional, dedicated hardware platform, like Yanai's microcomputer, was traditionally employed for this fixed dynamic range control. Yanai follows this rule by employing a fixed threshold value, V_1, for controlling pixel reset functionality. When a pixel voltage exceeds the threshold voltage value, V_1, Yanai resets the pixel. The value of the threshold value, V_1, is set by Yanai to be close to the pixel saturation voltage, V_{sat}, to produce a high signal/noise ratio for the pixel array (Col. 4, lines 31-33). There is thus no flexibility in adjusting Yanai's pixel reset function to adjust the

dynamic range of Yanai's imager; the dynamic range is fixed by Yanai's threshold voltage value, V_1.

In contrast, the invention provides a charge integration controller that can generate pixel-specific integration control signals based on a user-specified dynamic range for an imager. The controller can therefore accommodate flexible dynamic range specifications that may change over time as a user observes performance of the imager system with given scene and illumination conditions. As stated in the instant specification: "The parameters of the integration control method of the invention are user-programmable and can be user-adjusted from frame to frame in real time," (p. 42, lines 20-22). Further, the pixel-specific control signal generation by the integration controller of the invention is carried out on-chip with a pixel array; i.e., the controller is monolithically integrated with the array. Conventionally, at the time of the invention, there simply was no provision for an integration controller monolithically integrated with a pixel array to accept a specification of dynamic range by an imager user and in response generate pixel-specific integration control signals based on the dynamic range specification. Yanai completely fails to teach or suggest such.

The Examiner suggested that Yanai describes an output interface circuit to produce output image data based on sense node electrical signals from the pixel array, referring to Yanai Col. 10, lines 40-51 and output circuit 12 of Yanai Fig. 8. While Yanai does provide an output interface circuit, it appears that such is provided outside of the pickup element 1 in Fig. 8; i.e., as explained above, it appears that such is not integrated with a pixel array in a semiconductor substrate as required by the claims.

The Examiner suggested that Yanai does not describe an input interface circuit for accepting an input of "predetermined signal amount" or "threshold value." Indeed, as explained above, Yanai sets a threshold value, V_1, that is not adjustable; Yanai's dynamic range is correspondingly not adjustable. But the

Examiner took Official Notice that "both the concept and advantages of providing for [an] imager system which include[s] [an] input interface to accept a dynamic range specification input are well known and expected in the art." The Examiner went on to assert that it would have been obvious to have in input interface circuit to accept a dynamic range specification input in Yanai so that the dynamic range of the image system could be adjusted more flexibly and widely.

The Applicants hereby traverse the Examiner's Official Notice, as prescribed by MPEP 2144.03 C. The Examiner must therefore support his Official Notice finding with documentary evidence in a next Office action or must withdraw the rejection in his next Office action, as required by 37 C.F.R. 1.104(c)(2). Official Notice that is unsupported by documentary evidence can only be taken by the Examiner when the facts asserted to be well-known are capable of instant and unquestionable demonstration as being well-known. MPEP 2144.03A makes clear that such facts must be capable of instant and unquestionable demonstration, as to defy dispute, as noted *in re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

The Applicants support for this traverse is as follows. The Examiner stated that it would be obvious to employ an input interface circuit in the Yanai system so that the dynamic range of the Yanai system could be adjusted more flexibly and widely. But the Yanai system does not provide the integration controller required by the claims that would enable a flexible dynamic range. The Examiner has failed to consider all of the required elements of the claims that enable a flexible dynamic range. As explained above, the invention provides a discovery of an integration controller design and a microfabrication process to produce an integration controller that can generate pixel-specific integration control signals based on a dynamic range specification from an input interface circuit and that is integrated in a semiconductor substrate with a pixel array and other imager system components.

Without the flexible integration controller of the invention, there is absolutely no motivation for an input interface circuit to accept a dynamic range specification. That is why, at the time of the invention, when imager dynamic range was conventionally held fixed, there was no motivation to employ an input interface circuit. Not only would the use of an input interface circuit for specifying dynamic range not be well-known and capable of instant and unquestionable demonstration as being well-known, it would not even have been suggested. The Official Notice by the Examiner is therefore misplaced, and is traversed by the Applicants, requiring the Examiner to support his Official Notice finding with documentary evidence in a next Office action or to withdraw the rejection in his next Office action, as required by 37 C.F.R. 1.104(c)(2).

In the same light, there is clearly no motivation for combining an input interface circuit to accept a dynamic range specification input with the system of Yanai. This is because Yanai's system employs only a fixed threshold value for controlling integration of pixels, and the Yanai imager dynamic range cannot be adjusted at all. Yanai provides absolutely no hint of motivation for employing an input interface circuit. An input interface would serve no purpose in the Yanai system, and therefore there is no motivation to combine an input interface with the Yanai system.

In contrast, the invention provides a discovery of an integration control technique and corresponding integration controller that can generate pixel-specific integration control signals based on a user-input dynamic range specification. As explained above, from frame to frame, a user can adjust a dynamic range input specification to cause the integration controller to generate new pixel-specific integration control signals. The Yanai teaching is simply devoid of any such technique or apparatus.

Finally, as stated above, the Examiner is required to consider the invention as a whole, and further cannot ignore particular elements of the claims,

MPEP 2141.02. The question under 35 U.S.C. §103 is not whether differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc., v. Aeroquip Corp.,* 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983). When the invention is properly considered as a whole, including all of the recited limitations of claim 1, there is provided an imager system having a pixel array, pixel access control circuitry, an input interface circuit, integration control circuitry, and an output interface circuit that are all provided in a semiconductor substrate and that are configured to accept a dynamic range specification input and generate pixel-specific integration control signals based on the dynamic range specification input. The invention clearly requires more than a simple combination of an input interface circuit and an imager. As recited in claim 1, in the imager system of the invention, there is provided integration control circuitry that is connected to generate pixel-specific integration control signals based on the dynamic range specification input provided by the input interface circuit. In other words, the control circuitry is connected such that when a user inputs a dynamic range specification, the integration control circuitry generates a corresponding pixel integration control signal. This aspect of the integration control circuitry recited in claim 1 was ignored by the Examiner. The Examiner is not permitted to ignore limitations of the claims, and must consider the invention as a whole.

When properly considered, it is clear that the Yanai system fails to teach or suggest this imager system provided by the invention and recited in the claims. The Official Notice asserted by the Examiner with reference to an input interface connected to accept a dynamic range input is misplaced and traversed by the Applicants. Still, any combination of an input interface with the Yanai system fails to provide the configuration of a integration control circuitry that generates pixel-specific integration control signals based on a dynamic range specification input. And no combination of such provides a system that is

altogether provided in a semiconductor substrate. The Applicants therefore request reconsideration of the rejections of claims 1-5, 7-10, and 14-18.

With regard to claim 2, the Applicants concur that Yanai's pixels enable production of a voltage signal; but this does not provide the missing features required by claim 1, from which claim 2 depends. With regard to claim 3, the Applicants concur that Yanai's pixels can be CMOS pixels; but this does not provide the missing features required by claim 1, from which claim 3 depends. With regard to claim 4, the Applicants concur that the pixel-specific integration control signals of Yanai are reset signals; but this does not provide the missing features required by claim 1, from which claim 4 depends.

With regard to claim 5, the Examiner suggests that Yanai's imager system includes an array of memory cells, with each memory cell corresponding to a specified pixel in a pixel array and connected to store from the integration controller an indication of the number of reset occurrences of the specified pixel during a given integration period. This is not the case. The Examiner points to a capacitor C1 included in each Yanai pixel, shown in Yanai Fig. 9. Yanai explains that the capacitor C1 is a "storage capacitor serving as a photoelectric converting element," (Col. 10, lines 7-8). In other words, capacitor C1 stores the charge that is photoelectrically converted by the pixel from illumination captured by the adjacent photodiode D1 in the pixel. The capacitor C1 does not store an indication of number of reset occurrences of a pixel, it stores the charge accumulated by the pixel. Yanai makes this clear at the passage cited by the Examiner, describing an operation to "voltage-convert electric charges stored in the photodiodes D1 and the storage capacitors C1 of all the pixels," (Col. 10, 46-48). It is well understood that the capacitor C1 in Yanai's pixel is actually a parasitic capacitor associated with the p-n junction of the photodiode - the capacitor is not an actual circuit element, but is shown as such for modeling

purposes in a circuit schematic. There is thus no array of capacitors in the manner suggested by the Examiner.

Yanai does not use the photodiode capacitor of each pixel to keep track of reset occurrences. Instead, Yanai keeps track of the number of reset occurrences of a specified pixel in a microcomputer 14: "A microcomputer 14 records the number of reset times..." (Col. 5, line 47).

In contrast, in the invention, a memory array 24, shown in Fig. 1 of the instant application, is employed to keep track of the number of reset occurrences of each pixel. As shown in Fig. 1, the memory array 24 interfaces with the integration controller 20, which also is connected to control the pixel array 12. Because the integration controller is monolithically integrated in a silicon substrate with the pixel array, a memory array is required to also be integrated in the substrate for the image system of the invention. Yanai employs an off-chip microcomputer that can store reset occurrence data for each pixel at the microcomputer itself. This is not the case for the imager system of the invention, and is not the memory cell reset storage paradigm required by claim 5.

All of claims 6-10 depend from claim 5. It has been demonstrated just above that Yanai fails to provide the array of memory cells required by claim 5, and therefore Yanai fails to meet that requirement also made by claims 6-10.

In the invention as required by claim 6, a memory cell array that is spatially separate from the pixel array is provided storing an indication of the number of reset occurrences, as shown in Fig. 1 of the instant application. But as just explained, Yanai keeps track in a microcomputer of the number of times each pixel in his array is reset.

The Examiner suggested that Yanai's pixel storage capacitor configuration, in view of the system of Shinohara et al., U.S. No. 5,587,738, (hereinafter

"Shinohara") provides the spatially separate memory cell array required by claim 6.

Based on the discussion above, it is abundantly clear that there is no motivation to combine Yanai and Shinohara teachings. Yanai keeps track of pixel reset occurrences by a microcomputer off-chip from a pixel array. Yanai therefore has absolutely no use for a memory cell array provided at any location, either in-pixel or spatially separate from a pixel array. The storage capacitors C1 in Yanai's pixels are employed for storing accumulated photoelectric charge for imaging a scene, and are not provided for keeping track of reset occurrences as required by the claims. Therefore, for any Shinohara memory cell configuration, there is no motivation to combine such with the Yanai system. Further, no proper combination of the Yanai and Shinohara provides the memory cell configuration required by the claims for tracking pixel reset occurrences.

Claim 7 requires that the output interface circuit includes an image data formatter that is configured to generate output image data based on pixel sense node signals and reset occurrence data from the memory cell array. Yanai does not employ a memory cell array for tracking reset occurrence data, and thus fails the requirements of claim 7 for generating output image data based on data from a memory cell array. As explained above, the storage capacitor C1 in each Yanai pixel is employed for storing photoelectric charge accumulated from a scene illumination, not for storing reset occurrence data as was suggested by the Examiner.

Claim 8 requires that an integration controller of the imager system include a comparator circuit corresponding to each column of the pixel array. Each comparator circuit is required to be connected to compare a sense node electrical signal of a selected pixel with a reference signal that is generated based on the dynamic range specification input. This comparison produces a

comparator output signal that is determinative of reset timing of the selected pixel.

As explained previously, the integration controller of the invention, including the comparator circuits of claim 8, is connected such that when a user inputs a dynamic range specification, the integration control circuitry generates a corresponding pixel integration control signal that in claim 8 is required to be a comparator reference signal. Claim 8 requires a connection such that the reference signal is generated based on a "dynamic range specification input," referring to the "dynamic range specification input" antecedent basis provided by claim 1, referring to the input interface circuit of the invention that enables a dynamic range specification input.

The Examiner pointed to Yanai Fig. 7 as teaching a comparator "CNP," and referred to Yanai Col. 7, lines 36-49 as teaching the requirements of claim 8. As-stated in that passage, Yanai's microcomputer generates a pulse for resetting a pixel based on the comparator CNP output, with the comparator supplied with the reference voltage, V_1 that is set by Yanai to be close to the saturation voltage, V_{sat}, of the pixel, as explained previously.

Yanai's fails to meet the requirements of claim 8 just as he fails to meet the requirements of claim 1: both claims require that an integration controller be connected to generate an integration control signal, e.g., the reference signal of claim 8, based on a dynamic range specification from the input interface circuit; Yanai entirely fails to provide such, and this aspect of the integration control circuitry recited in claim 8 was ignored by the Examiner. As explained previously, there is clearly no motivation for combining an input interface circuit to accept a dynamic range specification input with the system of Yanai. This is because Yanai's system employs only a fixed threshold value, V_1, that is permanently set to be close to the pixel saturation voltage, V_{sat}, for controlling integration of pixels, and the Yanai imager dynamic range cannot be adjusted at

all. Yanai provides absolutely no hint of motivation or enabling teaching for an adjustable dynamic range. Thus, Yanai fails to meet the requirements of claim 8 as with claim 1.

Claim 9 requires that the integration controller of the invention be configured to generate integration control signals for a selected pixel based on output signals from a corresponding comparator to permit integration of the selected pixel during at least one of a plurality of integration slots. The integration slots are of successively shorter durations and all integration slots have a common end time. The durations of the integration slots are defined for a given imager integration period based on the dynamic range specification input.

The Examiner referred to Yanai Fig. 6 to suggest that Yanai teaches the requirements of claim 9.

Claim 9 requires several integration slot features:

- A plurality of integration slots must be provided
- The integration slots must be of successively shorter duration
- All integration slots must have a common end time
- The durations of the integration slots must be defined based on a dynamic range specification input

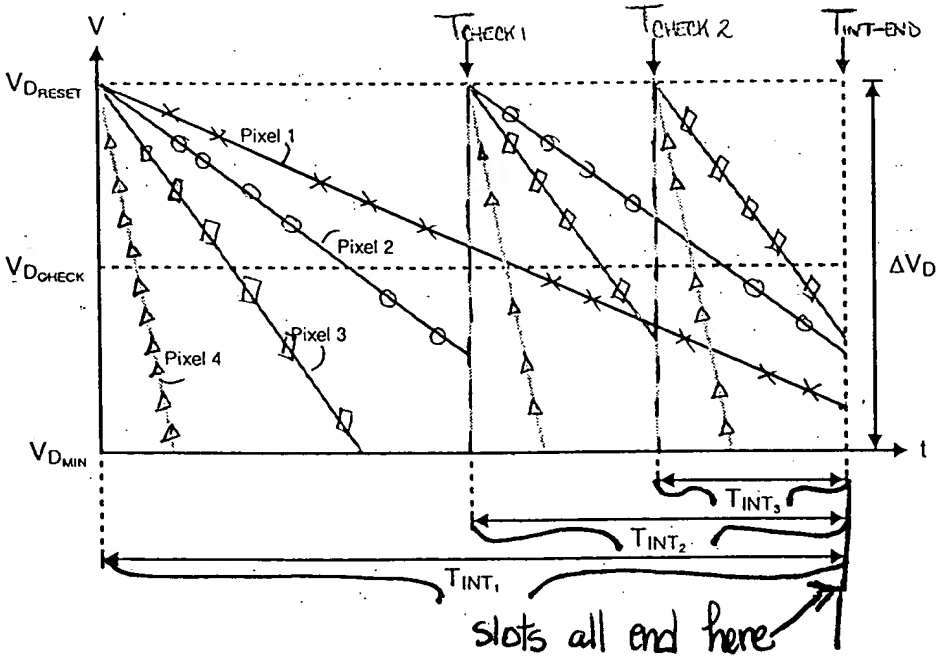
For ease of understanding, these features are described below with reference to the instant specification and Fig. 3 of the instant application, reproduced below. In Fig. 3 is shown the evolution of integrating charge for four pixels during an integration period, as described in the instant specification at pp. 15-20. Prior to the integration period, the total integration period is divided into a number of integration time slots, e.g., three slots: T_{INT1}, T_{INT2}, T_{INT3}. The integration slots all end at the same time - $T_{INT-END}$ as shown in the graph. The integration slots are of successively shorter durations. The first slot, T_{INT1} is the

longest; the second slot, T_{INT2}, is shorter, starting later than the first slot; and the third slot, T_{INT3}, is the shortest of all. The durations of the slots are based on a user-specified dynamic range input. For example, a dynamic range expansion factor K can be input to specify a ratio of the duration of the longest integration time slot and the duration of the shortest integration time slot, as explained with reference to Expression (8) of the instant application on p. 22.

As explained in detail below with regard to claim 19, during each of the integration slots, there is provided a check time, e.g., T_{CHECK1} and T_{CHECK2} in Fig. 3, at which it is determined for each pixel if that pixel has previously or will in the future saturate during a given integration slot. So the integration slots are set up prior to the integration period, with the intermediate check times likewise set up prior to the integration period, to enable implementation of the intermediate check times and pixel control decisions made at each check time.

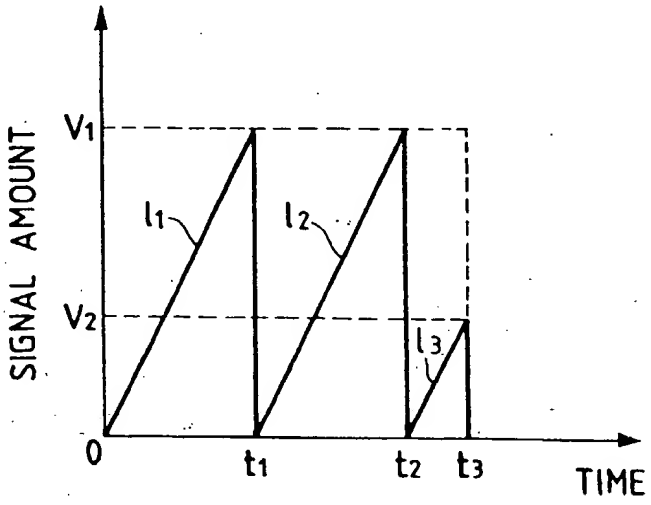
FIG. 3

X - Pixel 1
O - Pixel 2
□ Pixel 3
△ Pixel 4



Now referring to Yanai's Fig. 6 plot of a pixel voltage evolution, the Examiner suggests that t_1, t_2 and t_3 refer to a plurality of integration slots. This is not the case. In Yanai's system, when an integrating pixel signal reaches a threshold voltage, V_1, the pixel is reset. In Yanai Fig. 6, t_1 and t_2 refer to times that a pixel was reset. But if a pixel never reaches the threshold voltage, V_1, the pixel is never reset, and no such reset times would then exist. So no integration slots are defined by Yanai as required by the claims; instead, Yanai simply resets a pixel whenever the pixel reaches a threshold voltage, and Fig. 6 indicates example times at which such reset occurs.

YANAI FIG. 6



If one were to consider the time periods between t_1, t_2 and t_3 in Yanai Fig. 6 as integration slots, such do not meet the requirements of claim 9. First, the durations t_1 and t_2 are the same, not successively shorter durations as required by claim 9. This is because as Yanai continues to reset a pixel, the duration before each reset will be identical since the integration is linear; the successively shorter duration slots required by the claim are not provided by Yanai. Further,

if t_1 is considered the end of a first integration slot, t_2 the end of a second integration slot, and t_3 the end of a third integration slot, then each of the three slots ends at different times, not at a common time as required by claim 9.

In addition, if one were to consider the time periods between t_1, t_2 and t_3 in Yanai Fig. 6 as integration slots, the duration of such are not defined by a dynamic range specification input as required by the claims; the durations are instead defined simply by the slope of the linear integration characteristic of the pixel. No user-specific dynamic range input sets the durations shown in Yanai Fig. 6 or the threshold voltage, V_1, as explained above.

The Examiner points to Yanai Col. 5, lines 55-67 as suggesting that the integration slot periods are based on a dynamic range specification input. This is not the case. This passages states that when a pixel signal reaches the threshold, V_1, the charge is reset, and then at the end of the standard integration period, the "charge storage end time" t_3, the charge storage ends. This ending of the integration period is the conventional end of, e.g., taking a picture with a camera, and has nothing to do with dynamic range, let alone a dynamic range specification input as required by claim 9. The Examiner has mischaracterized this operation of the Yanai pixel. Yanai neither teaches nor makes a hint of suggestion of the pixel integration slot features required by claim 9.

Claim 10 depends from claim 9 and therefore includes all of the limitations required by claim 9. Claim 10 further requires that at least 3 integration slots be provided. The Examiner suggested that t_1, t_2 and t_3 refer to a plurality of integration slots in Yanai Fig. 6. As just explained, this is not the case. Duration t_3 refers to the end of the pixel integration, i.e., the end of a snapshot; durations t_1 and t_2 refer to times that Yanai resets a pixel; no prespecified integration slots are defined as required by the claims.

Claim 18 is here discussed because like claim 10, claim 18 depends from claim 9 and therefore includes all of the limitations of claim 9. Claim 18 requires that the dynamic range specification that is accepted by the input interface circuit be a specification of a duration ratio between successively started integration slots for a given integration period. Referring to Fig. 3 above from the instant application, claim 18 requires acceptance of an input that specifies, e.g., the ratio of T_{INT2}/T_{INT1}, which is the ratio of the duration of the second slot, T_{INT2}, to the duration of the first slot, T_{INT1}. As explained above, each successive integration slot is of a shorter duration, and therefore successive durations can be specified by a ratio.

The Examiner suggested that Yanai discloses a duration ratio between successively started integration slots at Yanai Col. 4, lines 45-64. At Yanai Col. 4, lines 45-64, it is explained that at the end of an integration period; i.e., at the end of the taking of an image snapshot or image frame, the total amount of charge that was stored in a pixel during that frame is computed. This stored charge, or signal, is computed as $V_i = V_1 \times t_s/t_1$, where V_i is the stored charge, t_s is the duration of the image frame integration period, and t_1 is the time when a pixel saturated during the image frame integration period, as shown in Yanai Fig. 2. This saturation time is determined by the microcomputer after the pixel reaches a threshold voltage, V_1, that is set close to the saturation voltage. As shown in Yanai Fig. 2, this computation equation is therefore employed at the end of an integration period to compute the output value of a pixel that saturated during the image frame integration period.

Clearly, this after-the-fact Yanai computation of output pixel value is not an input specification of the duration of successive integration slots as required by the claim. As explained above, Yanai fails to teach the use of any integration slots whatsoever. Instead, at the end of an integration period, Yanai's microcomputer determines the time at which a pixel saturated during the

integration period. In one Yanai embodiment, with reference to Fig. 2 just described, the ratio of that measured saturation time and the image frame integration period is computed after the integration period has ended. This computation after-the-face is not an input specification of the durations of successive integration slots as required by the claim.

Yanai's Fig. 2 makes clear that the even if the t_s and t_1 times in the plot were considered to be integration slots, they do not correspond to the integration slots of the claims. In Fig. 2, there is a longer duration between t_1 and t_s than there is between 0 and t_1, and the claims require that the integration slots be of successively shorter duration.

Claims 11-13 all depend from claim 1 and therefore include all of the limitations of claim 1. Claim 11 further requires that the output interface circuit include a correlated double-sampling circuit that is configured to convert pixel sense node signals from single-ended to differential output and to remove any pixel reset level from the sense node signals. Claim 12 requires that the output interface circuit further include an analog-to-digital converter that is configured to digitize pixel sense node signals. Claim 13 requires that an array of analog-to-digital converters be provided with a multiplexer connected to this array for directing pixel sense node signals to a selected converter in the array of converters.

The Applicants concur that Lee describes the use of a correlated double-sampling circuit and the use of an analog-to-digital converter or array of converters in connection with the output of pixel sense node signals. But Lee does not fill in the many features missing from Yanai and required by claims 11-13 as-dependent from claim 1, and no combination of Lee and Yanai does so. For brevity, the arguments presented above with regard to claim 1 are not here repeated, but as explained previously, Yanai fails to teach or suggest required features of the imager system of claim 1.

Claims 14-17 all depend from claim 1 and therefore require all of the limitations of claim 1. Claim 14 further requires that the input interface circuit be connected to accept a specification of a sub-array of pixels to be controlled in the pixel array. Here the integration control circuitry is connected to independently access a selected pixel in the sub-array of pixels. Claim 15 requires that the input interface circuit be connected to accept a specification of a number of pixels to be controlled in the pixel array. Here the integration control circuitry is connected to independently access a selected pixel in the number of pixels specified. Claim 16 requires that the input interface circuit be connected to accept a specification of a frame rate at which images are to be produced. Here the integration control circuitry is connected to impose an imager integration period based on the frame rate specification. Claim 17 requires that the input interface circuit be connected to accept a specification of sense node electrical signal digitization resolution with the output interface circuit here including an image data formatter that is configured to generate digitized output image data based on sense node electrical signals and the digitization resolution specification.

The Examiner suggested with regard to claims 14-17 that Yanai discloses all subject matter as discussed "with respect to same comment as with claim 1." The Applicants here assume that the Examiner is referring to his position that Yanai does not teach or suggest an input interface circuit, with the Examiner taking Official Notice that such would be well known and expected in the art.

As stated previously, the Applicants traverse the Examiner's Official Notice, as prescribed by MPEP 2144.03 C. The Examiner must therefore support his Official Notice finding with documentary evidence in a next Office action or must withdraw the rejection in his next Office action, as required by 37 C.F.R. 1.104(c)(2). Official Notice that is unsupported by documentary evidence can only be taken by the Examiner when the facts asserted to be well-known are capable

of instant and unquestionable demonstration as being well-known. MPEP 2144.03A makes clear that such facts must be capable of instant and unquestionable demonstration, as to defy dispute, as noted *in re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

The Examiner stated that it would be obvious to employ an input interface circuit in the Yanai system so that the dynamic range of the Yanai system could be adjusted more flexibly and widely. But the Yanai system does not provide the integration controller required by the claims that would enable a flexible dynamic range. The Examiner has failed to consider all of the required elements of the claims that enable a flexible dynamic range. As explained above, the invention provides a discovery of an integration controller design and a microfabrication process to produce an integration controller that can generate pixel-specific integration control signals based on a dynamic range specification from an input interface circuit and that is integrated in a semiconductor substrate with a pixel array and other imager system components.

Without the flexible integration controller of the invention, there is absolutely no motivation for an input interface circuit to accept a dynamic range specification. That is why, at the time of the invention, when imager dynamic range was conventionally held fixed, there was no motivation to employ an input interface circuit. Not only would the use of an input interface circuit for specifying dynamic range not be well-known and capable of instant and unquestionable demonstration as being well-known, it would not even have been suggested. The Official Notice by the Examiner is therefore misplaced, and is traversed by the Applicants, requiring the Examiner to support his Official Notice finding with documentary evidence in a next Office action or to withdraw the rejection in his next Office action, as required by 37 C.F.R. 1.104(c)(2).

In the same light, there is clearly no motivation for combining an input interface circuit to accept a dynamic range specification input with the system of

Yanai. This is because Yanai's system employs only a fixed threshold value for controlling integration of pixels, and the Yanai imager dynamic range cannot be adjusted at all. Yanai understandably provides absolutely no hint of motivation for employing an input interface circuit. An input interface would serve no purpose in the Yanai system, and therefore there is no motivation to combine an input interface with the Yanai system.

In contrast, the invention provides a discovery of an integration control technique and corresponding integration controller that can generate pixel-specific integration control signals based on a user-input dynamic range specification. As explained above, from frame to frame, a user can adjust a dynamic range input specification to cause the integration controller to generate new pixel-specific integration control signals. The Yanai teaching is simply devoid of any such technique or apparatus.

Finally, as stated above, the Examiner is required to consider the invention as a whole, and further cannot ignore particular elements of the claims, *MPEP 2141.02*. The question under 35 U.S.C. §103 is not whether differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc., v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983). When the invention is properly considered as a whole, including all of the recited limitations of claim 1, there is provided an imager system having a pixel array, pixel access control circuitry, an input interface circuit, integration control circuitry, and an output interface circuit that are all provided in a semiconductor substrate and that are configured to accept a dynamic range specification input and generate pixel-specific integration control signals based on the dynamic range specification input. The invention clearly requires more than a simple combination of an input interface circuit and an imager. As recited in claim 1, in the imager system of the invention, there is provided integration control circuitry that is connected to generate pixel-specific

integration control signals based on the dynamic range specification input provided by the input interface circuit. In other words, the control circuitry is connected such that when a user inputs a dynamic range specification, the integration control circuitry generates a corresponding pixel integration control signal. This aspect of the integration control circuitry recited in claim 1 was ignored by the Examiner. The Examiner is not permitted to ignore limitations of the claims, and must consider the invention as a whole.

Each of claims 14-17 makes specific requirements of the input interface circuit of claim 1, as recited above. But because Yanai does not teach or even hint at an input interface circuit, there is no teaching or suggestion by Yanai of an input interface circuit having the connections required by claims 14-17. As with claim 1, Yanai fails to meet the requirements of claim 14-17, including, respectively, a pixel sub-array indication input; an indication of number of pixels to be controlled; a frame rate input; and a digitization resolution input.

We now turn to the method of claim 19. As recited in claim 19, the invention provides a method for controlling charge integration of a plurality of photosensitive, charge integrating pixels of the pixel array described above and in claim 1, for capturing illumination of a scene to be imaged during an integration period. That is, each pixel includes a photogenerated charge accumulation region and a sense node at which an electrical signal, indicative of pixel charge accumulation, can be measured without discharging the accumulation region.

In the method of the invention, as recited in claim 19, in a step (A), a plurality of integration slots are provided for an integration period, with all of the integration slots ending with the end of the integration period. A first integration slot is defined to begin with the start of the integration period. Each integration slot following the first slot is of a successively shorter duration. In a step (B), charge integration of each pixel in the pixel array is initiated for the integration period and the first integration slot. Then, in a step (C), for any current

integration slot except a last integration slot, at an intermediate time during the current integration slot, the sense node electrical signal of each pixel for which the current integration slot was initiated is evaluated to determine if that pixel will saturate during the current integration slot. This saturation evaluation is based on the electrical signal range characteristic of that pixel and the ratio of duration of a next succeeding integration slot to duration of the current integration slot.

In a step (D), any pixel for which the integration evaluation indicates pixel saturation during the current integration slot is reset. In a step (E), continued integration to the end of the current integration slot is permitted for any pixel for which the integration evaluation does not indicate saturation during the current integration slot, and initiating a next succeeding integration slot for any reset pixel.

In a step (F), the steps (C) to (E) are repeated until the end of the integration period and the last integration slot is reached. Then in a step (G), output image data is produced for each pixel based on sense node electrical signals from that pixel and an indication of number of integration slots for which that pixel was initiated during the integration period.

The Examiner suggested that Yanai discloses the charge integration control method of claim 19, and refers to his comments regarding claim 9 above, with regard to Yanai Fig. 6.

First considering the requirements of claim 19 with the aid of Fig. 3 above from the instant application, claim 19 requires several integration slot features:

- A plurality of integration slots must be provided
- Each integration slots must be of a successively shorter duration
- All integration slots must end at the integration period end

In Fig. 3 of the instant application, reproduced above, is shown the evolution of integrating charge for four pixels during an integration period, as described in the instant specification at pp. 15-20. As recited in claim 19 at step (A), an integration period is divided into a number of integration time slots, e.g., three slots: T_{INT1}, T_{INT2}, T_{INT3}. The integration slots all end at the same time - $T_{INT-END}$ as shown in the graph. The integration slots are of successively shorter durations. The first slot, T_{INT1} is the longest; the second slot, T_{INT2}, is shorter, starting later than the first slot; and the third slot, T_{INT3}, is the shortest of all.

As recited in claim 19 at step (B), charge integration of all pixels, e.g., pixels 1-4 in Fig. 3, is initiated at the start of the first integration slot, T_{INT1}. Then, as recited in steps (C-D), during each integration slot except the last, a check time, e.g., T_{CHECK1} in Fig. 3, is imposed. At each check time, it is determined if a pixel will saturate at any time during that integration slot, i.e., it is determined if a pixel has previously saturated or will saturate at some later time during the current slot. If this is found to be the case, then that pixel is reset. In the example of Fig. 3, pixels 2, 3, and 4 are reset at T_{CHECK1}. It is found that pixels 3 and 4 saturated previously, before the check time, and it determined, based on integration slope, that pixel 2 will saturate at a time after the check time. Pixel 1 is determined to not saturate and therefore is permitted to integrate through to the end of the first integration slot, as recited in step (E).

Then in step (F), during a second integration slot, pixels 2-4 again begin integrating. At an intermediate check time, T_{CHECK2}, it is determined if any pixels have saturated or will later saturate during that integration slot. In the example of Fig. 3 it is determined that pixel 4 has previously saturated and so is reset. It is also determined that pixel 3 will saturate at a later time, and therefore is reset. Pixel 2 is allowed to continue integrating to the end of the second integration slot because it is determined that pixel 2 will not saturate during that slot. Then during a third integration slot, pixels 3-4 again begin

integrating, and continue to do so to the end of the third integration slot; no check time is imposed on the final integration slot. Finally, in step (G) output image data is produced based on an indication of the number of integration slots that were initiated for a pixel during the integration period.

Now referring to Yanai's Fig. 6 plot of a pixel voltage evolution, reproduced above, the Examiner suggests that t_1, t_2 and t_3 refer to a plurality of integration slots. This is not the case. When an integrating pixel signal reaches the threshold voltage, V_1, the pixel is reset. This could occur at any time and is not controlled by a previous definition of integration slot duration. In Yanai Fig. 6, t_1 and t_2 refer to times that a pixel was reset. But if the pixel never reaches the threshold voltage, V_1, the pixel is never reset. So no integration slots are defined by Yanai as required by the claims; instead, Yanai simply resets a pixel whenever the pixel reaches a threshold voltage.

In contrast, in the method of the invention, as recited in step (C), it is determined if a pixel will saturate at any time, previous to the check time or at a future time after the check time, during a current integration slot, not if a pixel already has saturated as Yanai does. So in Fig. 3, at the first check time, T_{CHECK1}, it is found that pixel 2 has not yet saturated but will saturate later in the first integration slot and therefore is reset. Similarly in Fig. 3, at the second check time, T_{CHECK2}, it is found that pixel 3 has not yet saturated but will saturate later in the second integration slot and therefore is reset. Yanai provides absolutely no teaching or hint at this predictive control technique of the invention. Instead Yanai simply resets a pixel immediately at the time that pixel saturates.

If one were to consider the time periods between t_1, t_2 and t_3 in Yanai Fig. 6 as integration slots, such do not meet the requirements of claim 19. First, the durations t_1 and t_2 are the same, not successively shorter durations as required by claim 19. This is because as Yanai continues to reset the pixel, the duration

before each reset will be identical since the integration is linear; the successively shorter duration slots required by the claim are not provided by Yanai. Further, if t_1 is considered the end of a first integration slot, t_2 the end of a second integration slot, and t_3 the end of a third integration slot, then each of the three slots ends at different times, not at a common time as required by claim 19.

The Examiner further referred to Yanai Col. 11, lines 22-54 with regard to the production of output image data for each pixel. This passage describes a control technique for accessing each pixel in an array for reading out the pixel values in the array. Nowhere does this passage teach or even mention the use of an indication of integration slot number for producing output image data - Yanai does not employ integration slots as required by the invention. It is not clear how the Examiner can suggest that this passage refers to the integration slot control technique of claim 19, and from the above, it is clear that Yanai neither teaches nor suggests the integration control technique of claim 19.

Claims 21-23 all depend from claim 19 and therefore include the limitations of claim 19. Claim 21 further requires that data stored in an array of memory cells be provided in a one-to-one correspondence with the pixel array, to reflect the number of times a pixel was reset during an integration period, with that reset number corresponding to the indication of the number of integration slots initiated for a pixel.

With regard to claim 21, the Examiner suggests that Yanai's imager system includes an array of memory cells, with each memory cell corresponding to a specified pixel in a pixel array and connected to store from the integration controller an indication of the number of reset occurrences of the specified pixel during a given integration period. This is not the case.

The Examiner points to a capacitor C1 included in each Yanai pixel, shown in Yanai Fig. 9. Yanai explains that the capacitor C1 is a "storage capacitor

serving as a photoelectric converting element," (Col. 10, lines 7-8). In other words, capacitor C1 stores the charge that is photoelectrically converted by the pixel from illumination captured by the adjacent photodiode D1 in the pixel. The capacitor C1 does not store an indication of number of reset occurrences of a pixel, it stores the charge accumulated by the pixel. Yanai makes this clear at the passage cited with regard to claim 5 by the Examiner, describing an operation to "voltage-convert electric charges stored in the photodiodes D1 and the storage capacitors C1 of all the pixels," (Col. 10, 46-48). The Examiner referred to Yanai Col. 7, lines 10-25. This passage also makes clear that each capacitor C1 stores accumulated pixel charge, with the passage referring to the completion of the storage operation to the capacitor. It is well understood that the capacitor C1 in Yanai's pixel is actually a parasitic capacitor associated with the p-n junction of the photodiode - the capacitor is not an actual circuit element, but is shown as such for modeling purposes in a circuit schematic. There is thus no array of capacitors in the manner suggested by the Examiner.

Yanai does not use the photodiode capacitor of each pixel to keep track of reset occurrences. Instead, Yanai keeps track of the number of reset occurrences of a specified pixel in a microcomputer 14: "A microcomputer 14 records the number of reset times..." (Col. 5, line 47).

In contrast, in the invention, a memory array 24, shown in Fig. 1 of the instant application, is employed to keep track of the number of reset occurrences of each pixel. As shown in Fig. 1, the memory array 24 interfaces with the integration controller 20, which also is connected to control the pixel array 12. Because the integration controller is monolithically integrated in a silicon substrate with the pixel array, a memory array is required to also be integrated in the substrate for the image system of the invention. Yanai employs an off-chip microcomputer that can store reset occurrence data for each pixel at the

microcomputer itself. This is not the case for the imager system of the invention, and is not the memory cell reset storage paradigm required by claim 21.

Claim 22 requires that at least 3 integration slots be provided. The Examiner suggested that t_1, t_2 and t_3 refer to a plurality of integration slots in Yanai Fig. 6. As just explained with regard to claim 10 previously, this is not the case. Duration t_3 refers to the end of the pixel integration, i.e., the end of a snapshot; durations t_1 and t_2 refer to times that Yanai resets a pixel; no specified integration slots are defined as required by the claims.

Claim 23 requires that the first integration slot be of a maximum duration, and a last integration slot be of minimum duration, with these durations determined based on an input dynamic range increase specification as a ratio, K, where $K = T_{INT,MAX}/T_{INT,MIN}$. In accordance with the invention, a user can input a dynamic range increase specification as a ratio and based on that ratio, the integration slot durations are determined such that each are successively shorter and the first and last durations meet the ratio criteria.

The Examiner referred to Yanai Col. 5, lines 16-30, describing a ratio t_1/t_s, as referring to the ratio required by claim 23. This is not correct. This Yanai passage refers to Yanai Fig. 2, which is a plot showing the time at which a pixel saturated prior to the end of an integration period, saturating at time t_1. The passage referred to by the Examiner describes a technique for a so-called "knee-correction" for this situation in which a pixel saturates prior to the end of an integration period. This process has absolutely nothing to do with setting the duration of successively shorter integration slots defined for an integration period. Instead, at the end of an integration period, this technique simply looks at the time at which a pixel saturated and divides that number by the duration of the integration period itself. This has nothing at all to do with setting up integration slots and fails to meet the claim requirements.

The Applicants therefore submit that Yanai fails to teach or suggest the invention as recited in any of the claims, and no proper combination of Yanai and Lee meets those requirements. The Applicants therefore submit that the claims are in condition for allowance, which action is requested.

If the Examiner has any questions or would like to discuss the claims, he is encouraged to telephone the undersigned Agent directly at his convenience at the phone number given below.

An Information Disclosure Statement accompanies this response.

Respectfully submitted,

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